

**Report on**

## **IEEE Technical Talk Series 2021**

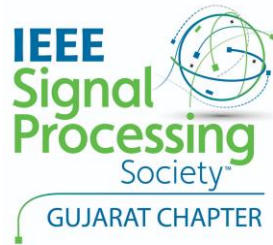


**Expert: Dr. Satyanarayana Bheesette**  
**June 26<sup>th</sup> 2021**

**Title: Advances in VLSI based Signal  
Processing and Applications**

**IEEE Signal Processing Society**

**Gujarat Section**



## Poster for the talk



Silver Oak University  
IEEE Student Branch



IEEE Signal Processing Society Gujarat Chapter  
presents

Expert Talk Series in collaboration with  
IEEE Bombay Section and IEEE SPS Silver Oak University SBC

*Advances in VLSI based signal  
processing and applications.*

June 26, 2021 | 10 AM IST

Scan to Register



Dr. Satyanarayana  
Bheesette,  
*Scientific Officer (H),  
TIFR, Mumbai*



<https://forms.gle/oZPVSpBwZfcAqs2b7>  
(WebEx link will be sent to registered participants)



## **Expert Profile**



### **Dr. Satyanarayana Bheesette** **Scientific Officer (H), TIFR, Mumbai**

Expert Profile: Dr. B. Satyanarayana did his B. Tech in Electronics and Communication Engineering from J.N.T. University, Hyderabad and Ph.D. in Physics from IIT Bombay. He is working in the Department of High Energy Physics, TIFR since 1983 – and is currently a Scientific Officer (H) and Coordinator of INO Project. He is also a Visiting Professor at the Applied Science Department of the American College, Madurai. His areas of interest include ‘Detectors and Instrumentation for high energy and nuclear physics experiments’. Dr. Satyanarayana has published about 250 research papers and proceedings in national and international journals and conferences, besides scores of invited talks. His very first paper won the best paper award by Institution of Electronics and Telecommunication Engineers (IETE). Recently he was honored with Homi Bhabha Award in Science Education (HBASE-2020) and has been selected as AICTE-INAE Distinguished Visiting Professor at the Symbiosis Institute of Technology, Pune. Dr. Satyanarayana is a Fellow of Institution of Electronics and Telecommunication Engineers (IETE) as well as Institute of Engineers (IE). He is a member of the Governing Council of Instrument Society of India (ISOI) as well as a Member of Indian Physics Association (IPA). He guided a large number of doctoral, master and undergraduate students. He served on many of doctoral and expert committees as well as academic councils, boards of studies and advisory boards on colleges, universities and many national organisations of eminence. He is on the editorial and refereeing teams of several prestigious science and engineering journals. Dr. Satyanarayana is a Senior Member of IEEE. He is currently an Executive Committee member and Chair of the IEEE Bombay Section. He previously served as the Vice Chair, Secretary, Chair of Technical and Professional Activities Committee of the Section as well as the Chair of its Signal Processing Society. He also served an Executive Committee member as

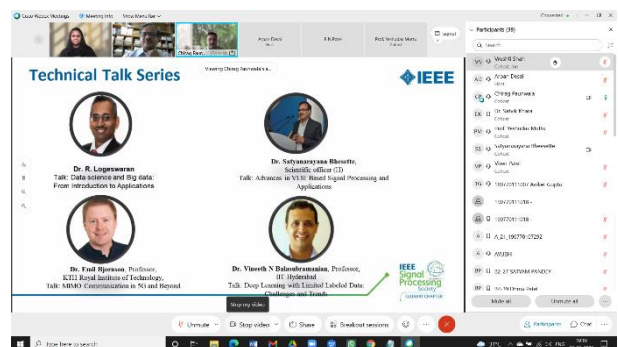
well as Vice Chair (Technical Activities) of the IEEE India Council. He won IEEE Bombay Section's Outstanding Volunteer Award for 2014 and IEEE Head Quarter's MGA Achievement Award for 2016.

## Glimpses of the Talk



**Activities under SPS, GS**

- Distinguished Lecturers (DL) and Distinguished Industry Speakers (DIS) Talks
- NETSP (New Trends in Signal Processing)
  - Flagship event in collaboration with DAICT, Gandhinagar, Gujarat, India
- Technical Talk Series
  - Intending to bring eminent experts in the field of Signal Processing, Machine/Deep learning, and Wireless Communications to provide a platform for budding engineers and professionals to be benefitted from the experts
- Women in Signal Processing
  - Aims to increase and promote visibility and recognition of women in signal processing fields
- YP Activities
  - This program is committed to help young professionals to evaluate their career goals, enhance early career skills and boost professional network



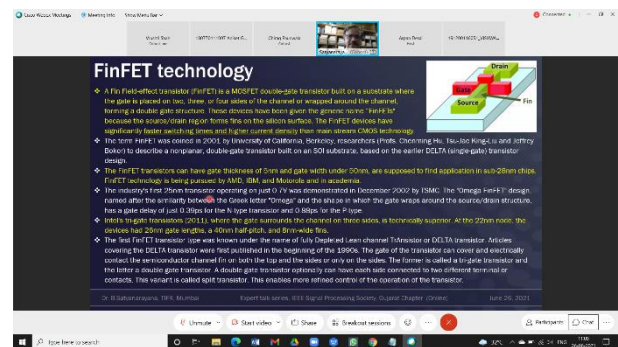
**Technical Talk Series**

- Dr. R. Logeswaran  
Talk: Data Science and Big data: From Introduction to Applications
- Dr. Subhasenara Bhattacharya  
Talk: Advances in VLSI Based Signal Processing and Applications
- Dr. Paul Srinivasan  
Talk: Deep Learning with Explicit Labeled Data
- Dr. Vireesh N. Balakrishnan  
Talk: Deep Learning with Explicit Labeled Data



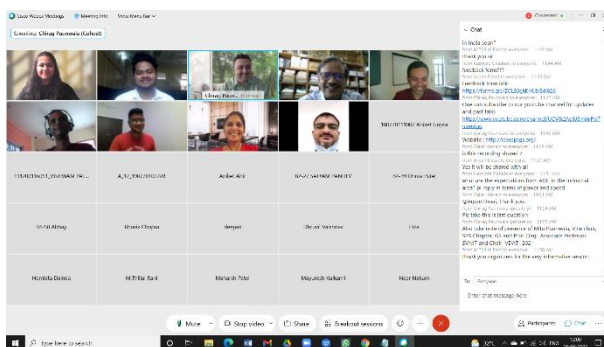
**Issues of sensor signal production**

- Duration**
  - Depends on the type of physical process exciting the sensor and details of signal production process in the external circuit
- Linearity**
  - Most sensors are characterized or chosen for linearity
  - Commercial components can expect non-linearity, offset and possible saturation
- Reproducibility**
  - Many signals are temperature dependent in magnitude - mobility of charges, other effects easily possible as well
- Ageing**
  - Sensor signals can change with time for many reasons
  - Natural degradation of sensor, variation in operating conditions, ambient parameters, etc.
  - All these issues mean that one should always be checking or calibrating measurements intended for accuracy, as best as one can.

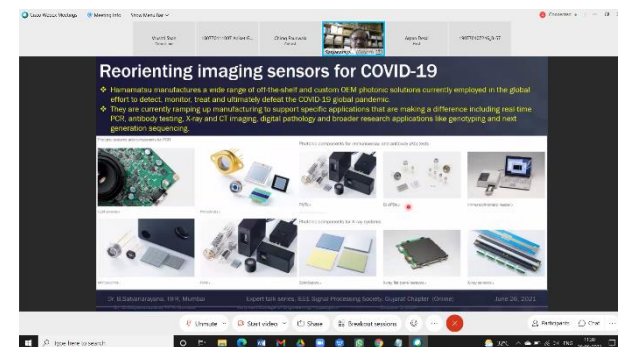


**FinFET technology**

- A Fin Field-effect transistor (FinFET) is a MOSFET double-gate transistor built on a substrate where the gate is placed on two, three or four sides of the channel or wrapped around the channel, forming a double-gate structure. These devices have been given the generic name FinFET because the source/drain region forms fins on the silicon surface. The FinFET devices have a superior barrier against leakage and higher current density than planar CMOS technology.
- The term FinFET was coined in 2003 by University of California, Berkeley researchers Prof. Ching-Hui Tsai, Ho-King Li and Jeffrey Bokor to describe a nonplanar, double-gate transistor built on an SOI substrate, based on the earlier DELTA (single-gate) transistor design.
- The FinFET transistors can have gate thickness of 20nm and gate width under 20nm, are supposed to find application in sub-20nm chips. FinFET technology is being pursued by AMD, IBM, and Motorola and is ascending.
- The industry first 28nm transistor operating on just 0.1  $\mu\text{m}$  was demonstrated in December 2009 by IMEC. The "Yin-yang bank" design named after the similarity between the Greek letter Omega and the shape in which the gate wraps around the source-drain structure, has a gate delay of just 0.3ns for the N-type transistor and 0.4ns for the P-type.
- Intel's single-gate transistors 28nm, where the gate surrounds the channel on three sides, is technologically superior. At the 28nm node, the devices had 25nm gate lengths, a 40nm half-pitch, and 8nm-wide fins.
- The first FinFET transistor was mass produced under the name of Intel's Intel Atom, a non-channel transistor or DELTA transistor. Articles covering the DELTA transistor were first published in the beginning of the 1990s. The gate of the transistor can cover and electrically contact the semiconductor channel from both the top and the sides or only on the sides. The former is called a triple-gate transistor and the latter a source-gate transistor. A double-gate transistor option is one where both ends connected to two different semi-circular contacts. This variant is called split transistor. This enables more refined control of the conduction of the transistor.



A grid of 12 video thumbnails showing various participants in a Zoom meeting. The thumbnails are arranged in two rows of six. The names of the participants are visible below each thumbnail.



**Reorienting imaging sensors for COVID-19**

- Hemeraeus manufactures a wide range of off-the-shelf and custom OEM photonic solutions currently employed in the global effort to detect, monitor, trace and ultimately defeat the COVID-19 global pandemic.
- They are currently ramping up manufacturing to support specific applications that are making a difference including real-time PCR antibody testing, Ray and CT imaging, digital pathology and broader research applications like genotyping and next generation sequencing.



## ✚ Memento Format



## ✚ Number of Participants

**Total: 143**

**IEEE Members: 51**

**NON-IEEE Members: 92**

**Report Prepared by: Dr. Satvik Khara**